# Effect of Split Gate Size on the Electrostatic Potential and 0.7 Anomaly within Quantum Wires on a Modulation-Doped GaAs/AlGaAs Heterostructure

L. W. Smith,[1,*] H. Al-Taie,[1,2] A. A. J. Lesage,[1] K. J. Thomas,[3,†] F. Sfigakis,[1] P. See,[4] J. P. Griffiths,[1] I. Farrer,[1,‡] G. A. C. Jones,[1] D. A. Ritchie,[1] M. J. Kelly,[1,2] and C. G. Smith[1]

[1]*Cavendish Laboratory, Department of Physics, University of Cambridge, J. J. Thomson Avenue, Cambridge CB3 0HE, United Kingdom*

[2]*Centre for Advanced Photonics and Electronics, Electrical Engineering Division, Department of Engineering, 9 J. J. Thomson Avenue, University of Cambridge, Cambridge CB3 0FA, United Kingdom*

[3]*Department of Electronic and Electrical Engineering, University College London, Torrington Place, London WC1E 7JE, United Kingdom*

[4]*National Physical Laboratory, Hampton Road, Teddington, Middlesex TW11 0LW, United Kingdom*

(Received 12 August 2015; revised manuscript received 13 February 2016; published 25 April 2016)

We study 95 split gates of different size on a single chip using a multiplexing technique. Each split gate defines a one-dimensional channel on a modulation-doped GaAs/AlGaAs heterostructure, through which the conductance is quantized. The yield of devices showing good quantization decreases rapidly as the length of the split gates increases. However, for the subset of devices showing good quantization, there is no correlation between the electrostatic length of the one-dimensional channel (estimated using a saddle-point model) and the gate length. The variation in electrostatic length and the one-dimensional subband spacing for devices of the same gate length exceeds the variation in the average values between devices of different lengths. There is a clear correlation between the curvature of the potential barrier in the transport direction and the strength of the "0.7 anomaly": the conductance value of the 0.7 anomaly reduces as the barrier curvature becomes shallower. These results highlight the key role of the electrostatic environment in one-dimensional systems. Even in devices with clean conductance plateaus, random fluctuations in the background potential are crucial in determining the potential landscape in the active device area such that nominally identical gate structures have different characteristics.

DOI: 10.1103/PhysRevApplied.5.044015

## I. INTRODUCTION

Low-dimensional devices which exhibit quantum-mechanical effects are routinely created using nanostructure gates on modulation-doped heterostructures. Often, devices with similar gate designs can display very different characteristics at cryogenic temperatures due to unpredictable local variations in the electrostatic landscape. In this paper, we investigate the impact of gate size on two important quantum properties of split-gate devices: the conductance quantization [1,2] and the occurrence of the 0.7 anomaly [3]. Experimental and theoretical techniques are used to determine the lateral and longitudinal potential profile in the one-dimensional (1D) channel. We find the 0.7 anomaly is governed by the electrostatic potential, regardless of gate size. However, fluctuations in the background potential due to ionized dopants often overwhelm the effect of changes in gate size in defining the potential landscape in the 1D channel.

The split gate is the simplest mesoscopic device that can be used to study how device behavior is affected by gate size. The conductance through a split gate [4] is quantized in multiples of $G_0 = 2e^2/h$ as a function of the voltage applied to the gates [1,2] due to the formation of 1D subbands. For an ideal 1D conductor, this quantization occurs as long as the transport remains ballistic. The effect of split-gate size can be investigated either by varying the lithographic dimensions [5–8] or by fabricating several split gates in close proximity which act in series to modify the potential of a single 1D channel [9–12]. So far, it has been shown that the split-gate voltage ($V_{SG}$) at which the conductance through the 1D channel is pinched off occurs closer to zero for longer and narrower devices [5,6]. Additionally, the quality of conductance quantization degrades as the gate length increases [8,13]. This latter effect is related to the higher probability of encountering an

*Corresponding author.
luke.smith@wisc.edu
Present address: Department of Physics, University of Wisconsin-Madison, Madison, WI 53706, USA.
†Present address: Department of Physics, Central University of Kerala, Riverside Transit Campus, Kasaragod 671 314, Kerala, India.
‡Present address: Department of Electronic & Electrical Engineering, University of Sheffield, Sheffield S1 3JD, United Kingdom.

 